PRIVATE LIMITED

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SUMMARY

- The Memorandum of understanding (MOU) is a statement of joint interest of both parties with the objective of fostering collaboration between the two institutions to promote academic collaboration and engagement. APS College of Engineering and eTech Prowess Private Limited wish to enter into a MOU wherein the Parties can explore possibilities of engagement & collaboration through the various engineering, technology & research capabilities offered by APS College of Engineering leading to drive integrated problem solving.
- The Parties intend to cooperate and focus their efforts on cooperation within the areas of skill based education, training, internship, placement, industrial visit, expert lecture, collaborative research projects etc.

NOW THEREFORE, IN CONSIDERATION OF THE MUTUAL PROMISES SET FORTH IN THIS MoU. THE PARTIES HERETO AGREE AS FOLLOWS

OBJECTIVES OF THE MOU:

The objective of this Memorandum of Understanding, interalia is:

- To promote interaction between APSCE, eTech Prowess in mutually beneficial areas.
- To provide Systematic Skill Development Program to the students of B.Tech (Electronic & Communication.
- To provide short term and long term internship to the students of B.Tech (Electronic & Communication.
- Value added engagement from both parties to enhance the skill level of students of APSCE and sharing industry best practices to students & faculties of B.Tech (Electronic & Communication) stream.
- To provide a formal basis for initiating interaction between APSCE and eTech Prowess .

PROPOSED MODES OF POTENTIAL COLLABORATION:

- APSCE and eTech Prowess may collaborate through one or more of the following projects or any such other projects as may be mutually agreed in between the Parties:
- Summer internship to B. Tech (E&C) Students of APSCE.
- Arranging project work for B. Tech (E&C) students.
- Upskilling of B. Tech (E&C) students in VLSI domain, explore opportunities for joint research programs undertaken by faculty and students of APSCE and eTech prowess personnel on topics identified by eTech Prowess.

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Bangalore-560 116

MEMORANDUM OF UNDERSTANDING

This Memorandum of Understanding ("MoU") is made on 18-04-2024 by and between:

APS COLLEGE OF ENGINEERING

And

eTech Prowess PVT LTD

APS College of Engineering, an entity incorporated under the laws of India represented by its Principal. (Hereafter referred to as "APSCE").

AND

ETECH PROWESS PVT LTD having its Registered Office 3rd Floor, Swathi Towers, BBL Layout, 3rd, Nagarabavi, East End Layout, JP Nagar 7th Phase, J. P. Nagar, Bengaluru, Karnataka 560078 hereinafter referred to as "eTech Prowess"):

nstitute and eTech Prowess Pvt. Ltd shall hereinafter be collectively referred to as "Parties" and ndividually as "Party"

WHEREAS

APS College of Engineering is specialized in providing value-added, holistic engineering educatio o Students at affordable costs, in a conducive academic ambiance, leading to personality development and intellectual growth.

Tech Prowess Pvt Ltd is an R&D Innovation Hub and educational institute which is focused on roviding quality embedded, Cloud Computing and VLSI education on the latest and cutting edge echnologies to students and also specializing in software/ hardware development, along with ong term courses for upskilling and Training. The goal of the company is to promote innovation, ntrepreneurship and also increasing employability quotient, thus making the students eady.

he Parties wish to cooperate with each other as per the terms and conditions. Enumerated in his MoU which is for constituting Centre of Excellence in Embedded Systems and VLSI in the remises of APSCE.

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	Embedded			
Training Materials & GIT repository codes	VLSI & Embedded	Rs. 5,00,000		Rs. 5,00,000
		Total Cost		Rs. 8,20,000

Scope of APSCE:

- APSCE will provide the space, Computer Systems, Internet connection, Projector, Projector screen etc.

Scope of eTech Prowess:

- eTech Prowess will invest on hardware and tools mentioned above.
- eTech Prowess will deploy dedicated Trainer for VLSI
- eTech Prowess will provide the Systematic Skill Development Programs (SSDP). Details of SSDP (week wise/semester wise modules) are furnished separately in the Annexure 1.
- eTech Prowess will conduct periodic evaluation and provide report to the APSCE Management about the progress.

Terms and Conditions:

- Curriculum for the SSDP program is mentioned in Annexure A
- Contract period and assurance to be awarded to eTech Prowess for minimum period of 5 years from APSCE
- Fee charged for the SSDP programs would be Rs.5,000 per student per year.
- Minimum of 100 students has to be committed by APSCE (including all semester students in an year combined) for training or equivalent amount of minimum Rs.5,00,000 of revenue assurance per year has to be committed by APSCE.
- Upon completion of the 5 years, all the applicable hardware by eTech Prowess will be transferred to APSCE.
- Payment terms: Invoice will be submitted within 7 days from the completion of training for each semester wise programs or as designed by APSCE Management Team. Payment to be made within 30 days from the date of invoice submission.

NOTE: Tools are subjected to renewal and non transferable.

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- Visits of eTech Prowess employees to the APSCE for conducting upskilling program, delivering lectures on industrial practices and trends.
- Workshops, conferences, and symposia with joint participation of the faculty and students of APSCE and eTech Prowess
- Short-term assignment, live projects to students in eTech Prowess.
- Any other appropriate mode of interaction agreed upon between APSCE and eTech Prowess

INFRASTRUCTURE TO BE PROVIDED BY APSCE FOR VLSI Training:

- 1000 Sq Ft Office space
- Computer system with internet connection
- Projector

INFRASTRUCTURE TO BE PROVIDED BY APSCE FOR Embedded Systems Training:

- 1000 Sq Ft Office space
- Computer system with internet connection
- Projector

INVESTMENT FROM eTtech Prowess :

Tools Required	Domain	Cost Per License	No. of Licenses	Total Cost for 5 years
Cadence EDA Tools related to Digital Physical Design Flow only	VLSI	Rs.1,00,00 per year	10	Rs. 50,00,000 per year
MATLAB & Simulink	Embedded	Rs. 74,000 per year	10	Rs. 37,00,000 per year
		Total Cost		Rs. 87,00,000 per year

Hardware Required	Domain	Cost Per Kit	No. of Kits	Total Cost
IOT Kits	Embedded	Rs.15,000	10	Rs.1,50,000
PC Components & Accessories	Embedded	Rs.1,000	20	Rs.20,000
Branding	VLSI &	Rs. 1,50,000		Rs. 1,50,000

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SIGNED IN DUPLICATE

This MoU is executed in duplicate with each copy being an official version of the Agreement and having equal legal validity.

BY SIGNING BELOW, the parties, acting by their duly authorized officers, have caused this Memorandum of Understanding to be executed, effective as of the day and year first above written.

On behalf of APSCE

Mr. Anand .
Principal
A.P.S. College of Engineering
Bangalore-560 114

Witness 1

Witness 2

On behalf of eTech Prowess

Mr. Srikanth BG
Director

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Phase, Bangalore 560078

CONFIDENTIALITY:

- The term "Confidential information" shall mean any information disclosed by one party ("Discloser") to the other ("Receiver"), pursuant to this MoU or otherwise, which is in written, graphic, machine readable or other tangible form and is marked as "Confidential" or 'Proprietary' or in some other manner to indicate its confidential nature. Confidential information may also include oral information disclosed by one party to the other, pursuant to this MoU, provided that such information is designated as Confidential at the time of disclosure and reduce to a written summary by the disclosing party, within 30 days after its oral disclosure, which is marked in a manner to indicate its confidential nature and delivered to the receiving party.
- For the term of this MoU, each party, shall treat as confidential all confidential information of the other party, shall not use such confidential information except as expressly set forth herein or otherwise authorized in writing, shall implement reasonable procedures to prohibit the disclosure, unauthorized duplication, misuse or removal of the other parties confidential information and shall not disclose such confidential information to any third party except as may be necessary and required in connection with the rights and obligations of such party under this MOU. Without limiting the foregoing, each of the parties shall use at least the same procedures and degree of care which it uses to prevent the disclosure of its own confidential information of like importance to prevent the disclosure of confidential information disclosed to it by other party under this MoU.

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eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	**Subtopics & Topic Details**	**Duration**	**Semester**
Digital Electronics	Number Systems: Binary, Decimal, Octal and Hexadecimal	week 1	2nd
	Number System Conversions: binary to others and others to binary	week 2	
	Logic Gates	week 3	
	Boolean algebra and laws	week 4	
	Classification of binary codes: BCD, excess-3, code conversions, alphanumeric codes	week 5	
	Canonical and Standard form, SOP & POS	week 6	
	K-Map Rules and Don't Care Conditions and minimization	week 7	
	Combinational circuit and Sequential circuit and delays	week 8	
	Adders, Comparators and Buffers	week 9	
	MUX and MUX as universal gate	week 10	
	DEMUX and DEMUX as universal gate	week 11	
	Encoder and priority encoder and Decoders	week 12	
	Latches, Flip-Flops, characteristic table & excitation table, Flip-Flop conversions	week 13	
	Synchronous Vs Asynchronous sequential circuits & Shift registers	week 14	
	Counters and Sequence generators, Frequency dividers and Sequence Detectors	week 15	

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Annexure A

eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	**Subtopics & Topic Details**	**Duration**	**Semester**
Introduction to ASIC Design Flow	Introduction to VLSI the holistics picture	week 1	1st
	Overview of VLSI Design Flow	week 2	
	ASIC Design Vs FPGA Design	week 3	
SC Physics	Semiconductor materials, properties and energy band diagram	week 4	
	Doping and Characteristics of p type and n type materials	week 5	
	Energy gap and pn junction diodes and formation of depletion layer	week 6	
	Diode Biasing and Characteristics curve	week 7	
	Zener diode Avalache diode		
CMOS Basics	Classification of MOSFETs & MOSFET applications	week 8	
	MOSFET Structure	week 9	
	Principle of operation and VI characteristics	week 10	
	CMOS Inverter structure and operation, Implementation of gates and boolean expressions	week 11	
	Stick diagram and layout	week 12	
	Introduction to process technology and clean room	week 13	
	Fabrication process steps	week 14	
	Short Channel Effects and Introduction to latest devices	week 15	

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eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	**Subtopics & Topic Details**	**Duration**	**Semester**
DFT	DFT introduction	week 1	4th
	Controllability and observability	week 2	
	Introduction to fault models	week 3	
	Fault model classification	week 4	
	Problems and Solutions	week 5	
	Testing methods	week 6	
	Scan Chain technique	week 7	
	BIST	week 8	
	PRNG and LFSR	week 9	
Linux	Creation of directory hierarchy, Execution of basic linux commands, Execution of linux file handling commands and hands on with Vi editor	week 10	
	Understanding and execution of file permission commands, Applying the short cut keys within a created file	week 11	
	Application, Usage of different modes of operation of GVIM and different modes of operation	week 12	
EDA Tools	Exploration of the EDA tools for physical design implementation	week 13	
	Investigation on "Xelium" & "Genus", EDA tool for several purposes	week 14	
	Examination of innovus tool for physical design flow	week 15	

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eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	Subtopics & Topic Details	Duration	Semester
Verilog	HDL and advantages and Levels of abstraction	week 1	3rd
	Modules, format and Verilog modeling styles	week 2	
	Module instantiation and Lexical conventions	week 3	
	Nets, wire, registers/variables, vectors, arrays and parameter constants	week 4	
	Ports and types and Verilog operators	week 5	
	RTL design examples and applications	week 6	
	RTL design examples and applications	week 7	
	Continuous process, procedural process, events, blocking and non-blocking assignment	week 8	
	Tasks, functions and timing control statements	week 9	
	Sequential, parallel, branching constructs and Looping constructs	week 10	
	Display system tasks	week 11	
	Test benches	week 12	
	RTL design and Verification examples and applications	week 13	
	RTL design and Verification examples and applications	week 14	
	RTL design and Verification examples and applications	week 15	

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	Powerplanning Goals and Steps in powerplanning	week 10	
	Powerplan Elements	week 11	
Placement	Goals of Placement and Steps involved in placement	week 12	
	Sanity checks before placement	week 13	
	Optimization Techniques for timing	week 14	
	Quality check after placement	week 15	

eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	**Subtopics & Topic Details**	**Duration**	**Semester**
CTS	Clock Tree	week 1	7th
	Signal Integrity	week 2	
	Impact on timing, area and power	week 3	
	Timing exceptions	week 4	
	CTS *optimization* and CTS *quality check*	week 5	
Routing	Goals of Routing and Stages in routing	week 6	
	Routing techniques	week 7	
	Sanity checks for Routing	week 8	
	Steps involved in routing	week 9	
Low Power Techniques	Need of low power techniqes and Issues due to power dissipation	week 10	
	Power reduction techniques I	week 11	
	Power reduction techniques II	week 12	
	Power reduction techniques III	week 13	
	Vital files of low power design	week 14	
	Report generation and Verification	week 15	

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eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	**Subtopics & Topic Details**	**Duration**	**Semester**
Synthesis	Synthesis Introduction	week 1	5th
	Optimization Techniques	week 2	
	Wire load model	week 3	
	Timing Exceptions	week 4	
	Timing Constraints	week 5	
	DRC Rules	week 6	
	DRV Rules	week 7	
STA	STA in ASIC Flow	week 8	
	Timing Path	week 9	
	Set-up and Hold time	week 10	
	Delay Calculation	week 11	
	Set-up and Hold check	week 12	
	Parasitics, RC delay corners	week 13	
	PVT conditions, operating conditions and environment	week 14	
	PVT variation, OCV	week 15	

eTech Prowess - Physical Design (PD) Course Curriculum			
Topic	**Subtopics & Topic Details**	**Duration**	**Semester**
Import Design	Import Design	week 1	6th
	Libraries	week 2	
	Inputs for Physical Design	week 3	
	Prilimiary Steps and Initial checks	week 4	
Synthesis	Goals of Floorplanning and Sanity checks before Floorplanning	week 5	
	Detailed study of specifications	week 6	
	Physical only cells	week 7	
	Macroplacement Guidelines	week 8	
	Checks after floorplanning	week 9	

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